



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,125	08/01/2003	Yiqun Lin	125.084US01	3083

7590 03/23/2006

Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339

EXAMINER

BOWERS, BRANDON

ART UNIT	PAPER NUMBER
----------	--------------

2825

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/633,125

Applicant(s)

LIN ET AL.

Examiner

Brandon W. Bowers

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-50 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

Claims 37-50 are objected to because of the following informalities: In order for a computer readable medium type claim to be considered statutory, an implication of execution of the medium must be present. An example of an acceptable preamble to claim 37 would be "A computer-readable medium including instructions for simulating the design of an integrated circuit from one process to another process that when executed on a computer cause the computer to perform a method comprising: ...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hall, US Patent No. 5,936,868.

In reference to claim 1, Hall teaches translating select device parameters in a first database associated with a first process to device parameters in a second database associated with a second process (column 3, lines 39-48), and displaying a design based on the device parameters in the second database (column 3, lines 54-57).

In reference to claims 2-5, Hall teaches wherein the select device parameters are resistance, capacitance, and geometry parameters and wherein selected parameters from the 1st circuit design are retained in the 2nd circuit design (column 7, line 21 – column 8 line 40).

In reference to claims 6-7, Hall teaches schematic design and layout displays (column 1, lines 50-60, column 2, lines 15-29, and column 3, lines 54-57).

In reference to claim 8, Hall teaches mapping mask layers (Figures 1A-5C).

In reference to claim 9, Hall teaches selectively adding extra interconnect layers (column 8, lines 33-40).

In reference to claim 10, Hall teaches preserving instance names between the 1st and 2nd databases (column 3, lines 39-48).

In reference to claim 11, Hall teaches checking and correcting grid and line mode automatically (column 2, lines 15-29).

Claims 1-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Yin, US Patent No. 6,298,469.

In reference to claim In reference to claim 1, Yin teaches translating select device parameters in a first database associated with a first process (Figures 1 and 3, 115, 115, 118, and 120) to device parameters in a second database associated with a second process (Figure 3, 303, 308), and displaying a design based on the device parameters in the second database (Column lines 19-60).

In reference to claims 2-5 and 8-10, Yin teaches converting cell placements and interconnectivity wires from one coordinate system to another and in so doing, a completely new database (physical, place & route and netlist) of the integrated circuit are created (generated) for new manufacturing process (column 4, lines 43 – 67).

In reference to claims 6-7 and 11-13, Yin teaches wherein the methodology is performed in a graphical interface environment with the ability to display the steps being performed (Column lines 19-60).

In reference to claim 14, Yin teaches setting translation options (Column 3, lines 23-42), reading original schematic and layout informations (Figures 1 and 3, 115, 115, 118, and 120), translating the schematic and layout informations (Figure 3, 303, 308) and outputting parameters of the translated schematic and layout informations (column 5, lines 4 –24).

In reference to claims 15-25, Yin teaches converting cell placements and interconnectivity wires from one coordinate system to another and in so doing, a completely new database (physical, place & route and netlist) of the integrated circuit are created (generated) for new manufacturing process (column 4, lines 43 – 67).

In reference to claims 26-27, Yin teaches creating and reading a configuration file wherein the configuration file comprises at least one of the functions in the group of functions comprising, mapping devices, mapping terminals, mapping mask layers, mapping parameters, inserting original device parameters, creating polarity and rotation, defining resistor and capacitor options, defining interconnect options and defining functions to be triggered after translation (column 4, lines 43 – 67).

In reference to claims 29-36 Yin teaches wherein the methodology is performed in a graphical interface environment with the ability to display the steps being performed (Column lines 19-60).

In reference to claims 37-50 drawn to a computer readable medium containing instruction for performing the methods rejected in claims 14-36 above, the same rejection applies.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hall, US Patent No. 5,936,868.

In reference to claims 12 and 13, Hall teaches claim 1 as described above. Hall further teaches displaying both the original and updated designs (column 3, line 54 – column 4, line 8). While Hall does not explicitly teach displaying both the original and updated designs side by side, it would have been obvious for one skilled in the art at the time of invention to display both the original and updated designs side by side because it would allow the user to see the changes made between the two designs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W. Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BWB


VUTHE SIEK
PRIMARY EXAMINER